IN THE CLAIMS

Claim 1 (original): An integrated circuit chip mounted on a leadframe, said leadframe having a plurality of segments, comprising:

a network of power distribution lines deposited on the surface of said chip over active components of said circuit;

said lines connected vertically to said components by metal-filled vias, and also to said segments by conductors; and

the majority of said lines patterned as straight lines between said vias and said conductors, respectively, thereby minimizing the distance for power delivery between a selected segment and one or more corresponding active components, to which said power is to be delivered.

Claim 2 (original): The chip according to Claim 1 further having said lines fabricated with a sheet resistance of less than 1.5 mΩ/□ and positioned to minimize parasitic electrical losses in power delivery between a selected segment and one or more corresponding active components, to which said power is to be delivered.

Claim 3 (original): The chip according to Claim 2 wherein said parasitic electrical losses include voltage drops during said power current flow, capacitances between said network and said active components, and inductances between network lines.

Claim 4 (previously presented): A semiconductor device wherein electrical parasitics are minimized by individualized power distributors deposited over active integrated circuit components, comprising:

a semiconductor chip having first and second surfaces;

an integrated circuit fabricated on said first chip surface, said circuit having active components, contact pads, at least one metal layer, and being protected by a mechanically strong, electrically insulating overcoat having a plurality of metal-filled vias to contact said at least one metal layer;

electrically conductive films deposited on said overcoat and patterned into a network of lines substantially vertically over said active components, said films in contact with said vias and having an outermost film of non-corrodible, metallurgically attachable metal;

said network patterned to distribute power current while minimizing parasitic electrical losses between said network and said active components;

said network further patterned to minimize silicon real estate consumed by power interconnections between said active components;

a leadframe having a chip mount pad, a first plurality of segments providing electrical signals, and a second plurality of segments providing electrical power and ground;

said second chip surface attached to said chip mount pad;

electrical conductors connecting said contact pads with said first plurality of segments; and

electrical conductors connecting said network lines with said second plurality of segments.

Claim 5 (original): The device according to Claim 4 wherein said chip is selected from a group consisting of silicon, silicon germanium, gallium arsenide, and any other semiconductor material customarily used in electronic device fabrication.

Claim 6 (cancelled)

Claim 7 (original): The device according to Claim 4 wherein said integrated circuit comprises multi-layer metallization, at least one of said layers made of pure or alloyed copper, aluminum, nickel, or refractory metals.

Claim 8 (original): The device according to Claim 4 wherein said overcoat comprises materials selected from a group consisting of silicon nitride, silicon oxynitride, silicon carbon alloys, polyimide, and sandwiched films thereof.

Claim 9 (original): The device according to Claim 4 wherein said leadframe is pre-fabricated from a sheet-like material selected from a group consisting of copper, copper alloy, aluminum, iron-nickel alloy, or invar.

Claim 10 (cancelled)

Claim 11 (original): The device according to Claim 10 wherein said encapsulation comprises a polymer compound fabricated in a transfer molding process.

Claim 12 (cancelled)

Claim 13 (original): The device according to Claim 4 wherein said lines and contact pads are attached to outside parts by solder balls.

Claim 14 (original): The device according to Claim 4 wherein said conductive films comprise a stack of stress-absorbing metal films under said outermost metallurgically attachable film.

Claim 15 (previously presented) The device according to Claim 4 wherein said electrical conductors are selected from a group comprising wire ball and stitch bonding, ribbon bonding, and soldering.

Claim 16 (original): The device according to Claim 14 wherein said stack of films comprise a layer of seed metal, promoting adhesion to said vias and inhibiting migration of overlying metals to said vias, at least one stress- absorbing metal layer, and an outermost metallurgically attachable metal layer.

Claim 17 (original): The device according to Claim 16 wherein said seed metal is selected from a group consisting of tungsten, titanium, titanium nitride, molybdenum, chromium, and alloys thereof.

Claim 18 (original): The device according to Claim 16 wherein said stress-absorbing metal layer comprises at least one layer selected from a group consisting of copper, nickel, aluminum, and alloys thereof.

Claim 19 (original): The device according to Claim 16 wherein said outermost metal layer is selected from a group consisting of pure or alloyed aluminum, gold, palladium, silver and platinum.

Claim 20 (original): The device according to Claim 4 wherein said conductors are bonding wires, bonding ribbons, or solder balls.

Claim 21 (original): The device according to Claim 20 wherein said bonding wire is selected from a group consisting of pure or alloyed gold, copper, and aluminum.

Claim 22 (original): The device according to Claim 20 wherein said solder ball is selected from a group consisting of pure tin, tin alloys including tin/copper, tin/indium, tin/silver, tin/bismuth, tin/lead, and conductive adhesive compounds.

Claim 23 (original): The device according to Claim 4 wherein said network of lines is electrically further connected to selected segments suitable for outside electrical contact.

Claims 24-28 (withdrawn)

Claim 29 (previously added): An integrated circuit chip mounted on a leadframe, said leadframe having a plurality of segments, comprising:

a network of power distribution lines deposited on the surface of said chip over active components of said circuit;

said lines comprising a stack including a stress-absorbing metal film;

said lines connected vertically to said components by metal-filled vias, and also to said segments by conductors; and

the majority of said lines patterned as straight lines between said vias and said conductors.

Claim 30 (previously added): The device of Claim 29, wherein said stack including a stress-absorbing metal film comprises an outermost metallurgically attachable film.

Claim 31 (previously added): The device of Claim 29, wherein said stack including a stress-absorbing metal film comprises a layer of seed metal, a stress-absorbing metal layer on said seed metal layer, and an outermost metallurgically attachable metal layer.

Claim 32 (previously added): The device of Claim 31, wherein said stress-absorbing metal layer comprises at least one layer selected from a group consisting of copper, nickel, aluminum, and alloys thereof.

Claim 33 (previously added): The device of Claim 31, wherein said seed metal is selected from a group consisting of tungsten, titanium, titanium nitride, molybdenum, chromium, and alloys thereof.

Claim 34 (previously added): The device according to Claim 31, wherein said outermost metal layer is selected from a group consisting of pure or alloyed aluminum, gold, palladium, silver and platinum.